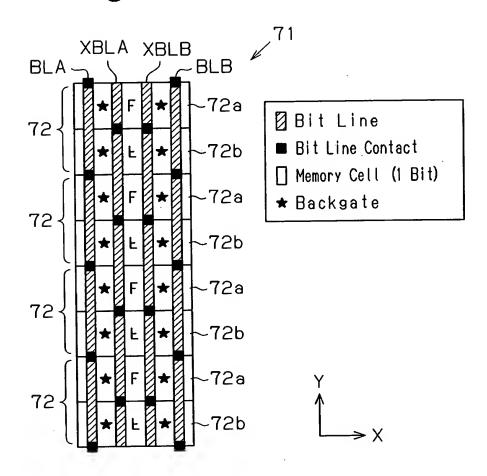
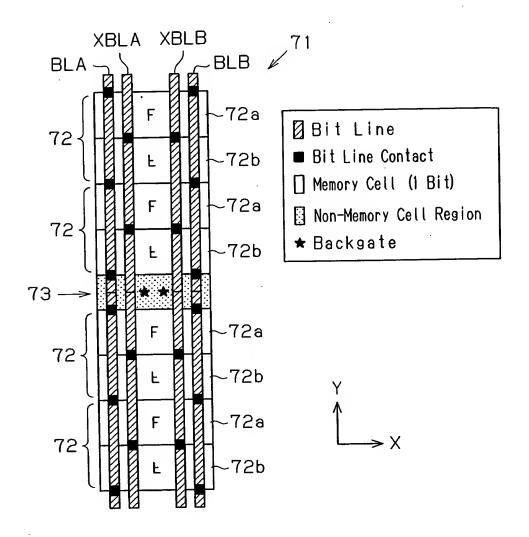
#### Fig 1 (Prior Art)



## Fig.2(Prior Art)



# Fig 3 (Prior Art)

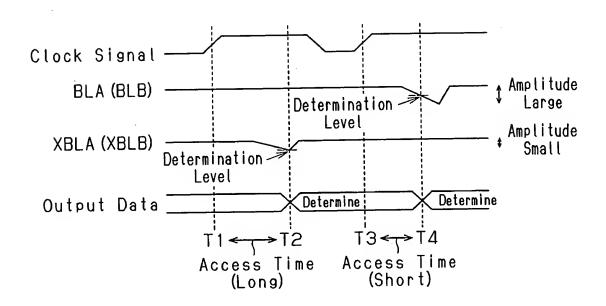


Fig.4

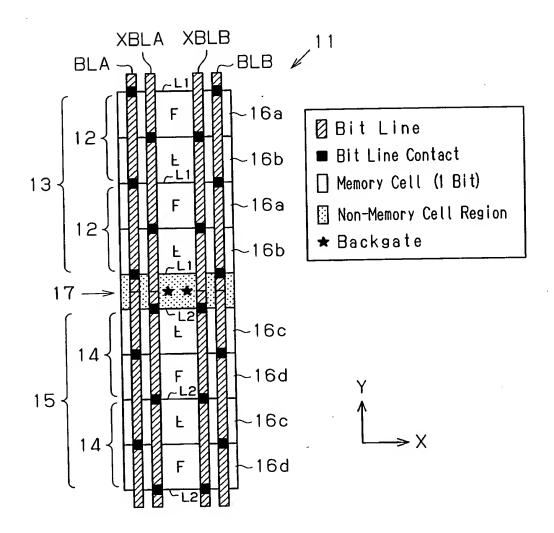
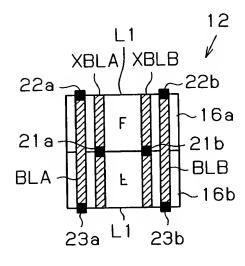


Fig.5A



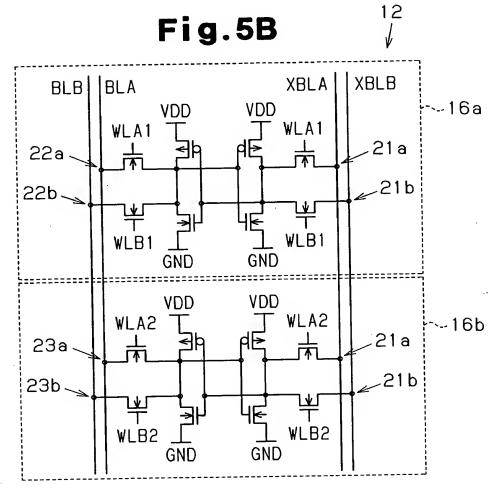
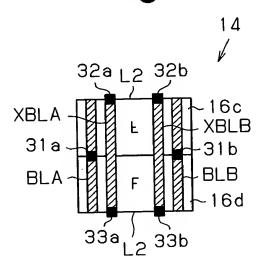


Fig.6A



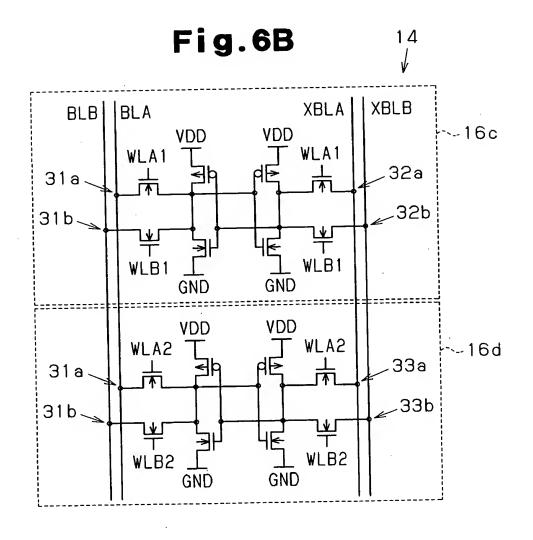
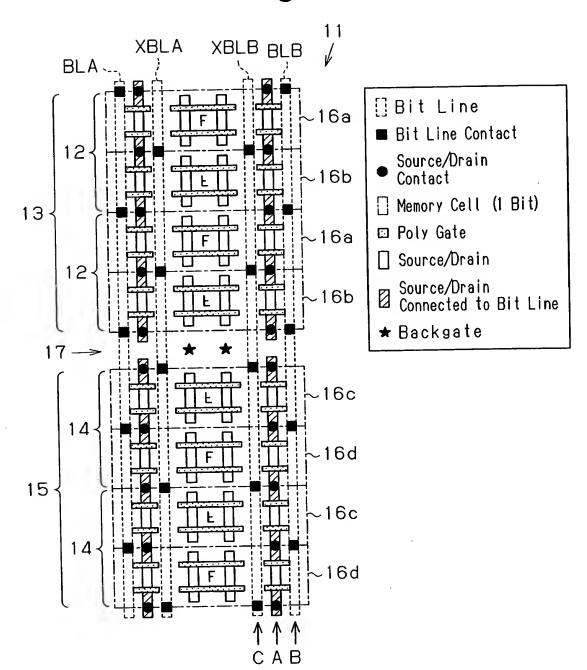


Fig.7



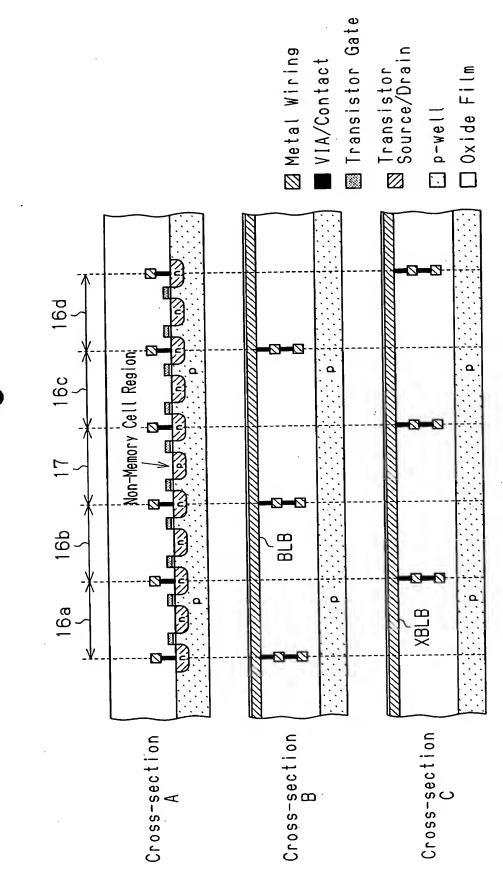


Fig.8

Fig.9

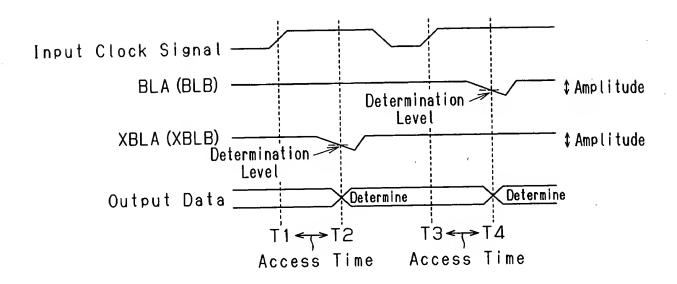
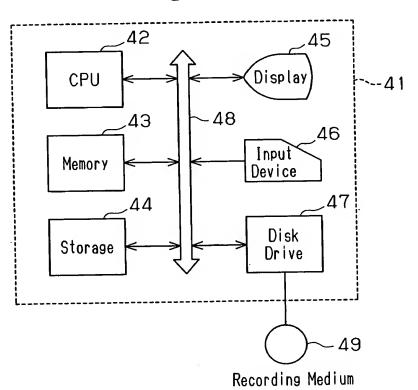


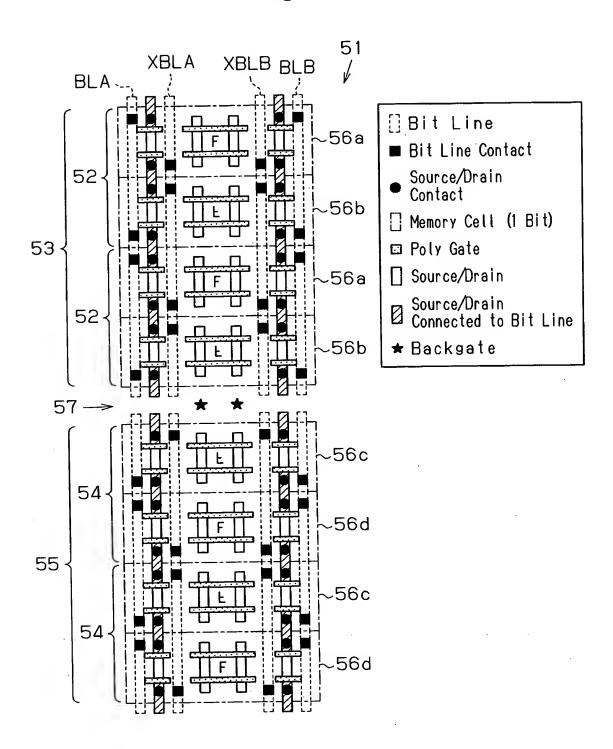
Fig.10



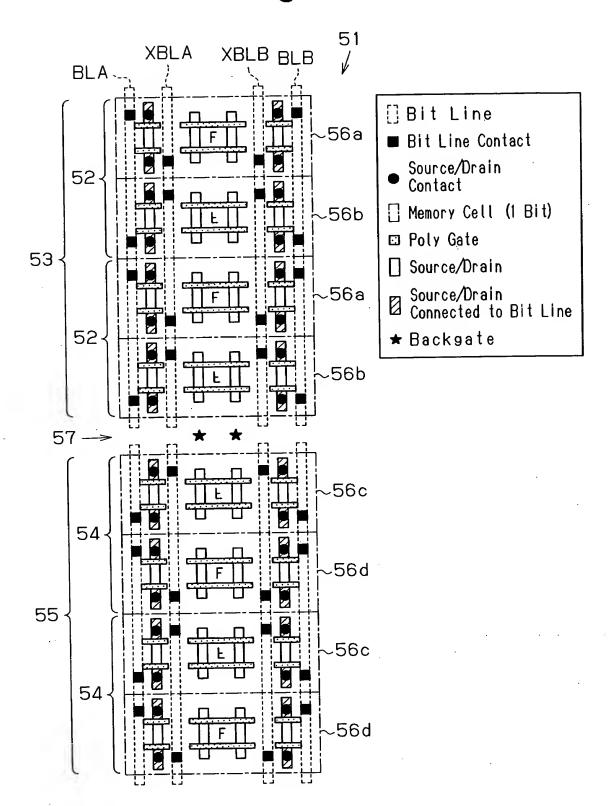
Inventor: Kenji KASUGA Title: Semiconductor Memory Device and Method for

Arranging Memory Cells
Attorney Docket No: 108075-00119

#### **Fig 11**



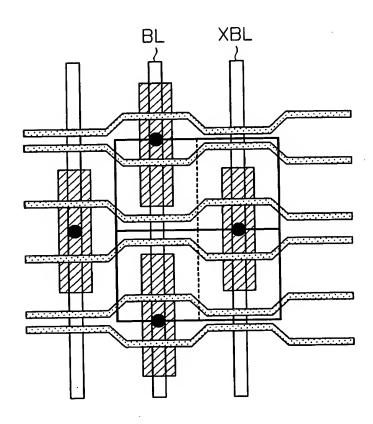
#### Fig.12



Inventor: Kenji KASUGA
Title: Semiconductor Memory Device and Method for
Arranging Memory Cells

Attorney Docket No: 108075-00119

### Fig 13



- Contact
- Source/Drain
- Poly Gate
- ☐ Metal Wiring
- ☐ Arrangement Unit (2 Bits)